IN THE CLAIMS

Please cancel Claims 9-38, 45-64, 68-112, and 121-154 without prejudice or disclaimer.

Claim 1 (previously presented): An electrical circuit comprising:

a low voltage transistor provided in a high voltage environment, said high voltage environment being characterized by a high supply voltage, said low voltage transistor containing a plurality of terminals, said low voltage transistor being designed to operate at a low cross terminal voltage, wherein said low cross terminal voltage is lower than said high supply voltage, one of said plurality of terminals of said low voltage transistor also receiving a voltage at least substantially equaling said high supply voltage, said low voltage transistor receiving and propagating an analog signal which potentially varies continuously with time.

Claim 2 (currently amended): The electrical circuit of claim 1, wherein said ~~said~~ analog signal comprises an input signal being processed by said electrical circuit such that said input signal can be processed quickly.

Claim 3 (original): The electrical circuit of claim 2, further comprising a second low voltage transistor provided at an output node of said electrical circuit.

Claim 4 (original): The electrical circuit of claim 3, wherein a bulk terminal of said second low voltage transistor is connected to a source terminal of said second low voltage transistor.

Claim 5 (original): The electrical circuit of claim 4, wherein said second low voltage transistor comprises a PMOS transistor.

Claim 6 (original): The electrical circuit of claim 3, further comprising a third low voltage transistor having a first terminal connected to said output node, a bulk terminal of said third low voltage transistor being connected to a voltage greater than said low voltage.

Claim 7 (original): The electrical circuit of claim 6, wherein a gate terminal of said third low voltage transistor is coupled to a clock signal having a high level greater than or equal to said low voltage.

Claim 8 (previously presented): The electrical circuit of claim 7, wherein said high level of said clock signal is substantially more than said low voltage to provide a high drive strength for said third low voltage transistor, and a low level of said clock signal is greater than or equal to voltage of said high level - a maximum permissible voltage level of said low voltage transistor.

Claims 9-38 (cancelled).

Claim 39 (previously presented): An electrical circuit comprising:

a low voltage transistor designed for operation at a low voltage and having a maximum permissible voltage, said low voltage transistor containing a plurality of terminals including a first terminal and a second terminal, said low voltage transistor being connected to a first higher voltage and said second terminal being connected to receive an analog signal which potentially varies continuously with time, wherein said

first higher voltage is greater than said low voltage, wherein a cross terminal voltage between said first terminal and each of the remaining terminals is constrained to not exceed said maximum permissible voltage, said low voltage transistor operating to propagate said analog signal.

Claim 40 (previously presented): The electrical circuit of claim 39, wherein said first higher voltage comprises a substantial fraction of a high supply voltage associated with a high voltage environment.

Claim 41 (original): The electrical circuit of claim 40, further comprising a high voltage transistor designed for operation at said high supply voltage.

Claim 42 (original): The electrical circuit of claim 41, wherein said low voltage transistor comprises a PMOS transistor, wherein a bulk terminal of said PMOS transistor is connected to a source terminal of said PMOS transistor, wherein both of said bulk terminal and said source terminal are coupled to receive a slightly less voltage than said high supply voltage.

Claim 43 (original): The electrical circuit of claim of claim 41, wherein said low voltage transistor comprises a PMOS transistor, wherein a bulk terminal of said PMOS transistor is connected to a voltage slightly higher than said low voltage.

Claim 44 (original): The electrical circuit of claim 43, wherein said bulk terminal is connected to 2.1V and said low voltage equals 1.8V.

Claims 45-64 (cancelled).

Claim 65 (previously presented): A device comprising:

a low voltage transistor in a high voltage environment, wherein said high voltage environment is characterized by a high supply voltage and a voltage equaling said high supply voltage is applied to one of the terminals of said low voltage transistor, another one of the terminals of said low voltage transistor being connected to receive an analog signal which potentially varies continuously with time, said low voltage transistor operating to propagate said analog signal; and

means for constraining cross terminal voltages of said low voltage transistor to substantially less than a maximum permissible voltage for which said low voltage transistor is designed, wherein said maximum permissible voltage is less than said high supply voltage.

Claim 66 (original): The device of claim 65, wherein said means for constraining does not contain a low voltage regulator which generates said low voltage from said high voltage.

Claim 67 (original): The device of claim 65, wherein said cross terminal voltages are constrained to not substantially more than a low voltage for which said low voltage transistor is designed.

Claims 68-112 (cancelled).

Claim 113 (previously presented): A method of implementing an electrical circuit, said method comprising:

providing a low voltage transistor in a high voltage environment, wherein said high voltage environment is characterized by a high supply voltage and a voltage equaling said high supply voltage is applied to one of the terminals of said low voltage transistor, another one of the terminals of said low voltage transistor being connected to receive an analog signal which potentially varies continuously with time, said low voltage transistor operating to propagate said analog signal; and

constraining cross terminal voltages of said low voltage transistor to substantially less than a maximum permissible voltage for which said low voltage transistor is designed, wherein said maximum permissible voltage is less than said high supply voltage.

Claim 114 (original): The method of claim 113, wherein said constraining is performed without using a low voltage regulator which generates said low voltage from said high voltage.

Claim 115 (original): The method of claim 113, wherein said cross terminal voltages are constrained to not substantially more than a low voltage for which said low voltage transistor is designed.

Claim 116 (previously presented): A method of implementing an electrical circuit with a high SNR and a high throughput performance, wherein said electrical circuit is designed to process an input signal and generate an output signal, said method comprising:

using a high supply voltage for said electrical circuit; and

providing a low voltage transistor in a path from said input signal to said output signal, wherein said low voltage transistor provides said high throughput performance and wherein said use of high supply voltage enables providing said high SNR, wherein said input signal comprises an analog signal.

Claim 117 (original): The method of claim 116, wherein said low voltage equals 3.3 V and said high supply voltage equals 1.8V.

Claim 118 (cancelled).

Claim 119 (original): The method of claim 116, wherein said output signal comprises an analog signal.

Claims 120-155 (cancelled).

Claim 156 (previously presented): The electrical circuit of claim 1, wherein said low voltage transistor operates in a saturation mode when propagating said input signal.

Claim 157 (previously presented): The electrical circuit of claim 1, wherein said low voltage transistor is comprised in an amplifier.

Claim 158 (previously presented): The electrical circuit of claim 1, further comprising a high voltage transistor being designed to operate at said high supply

voltage, said high voltage transistor and said low voltage transistor being comprised in a single integrated circuit.

Claim 159 (previously presented): The electrical circuit of claim 39, wherein said low voltage transistor is designed to operate in a saturation mode when propagating said analog signal.

Claim 160 (previously presented): The electrical circuit of claim 159, wherein said low voltage transistor is comprised in an amplifier.

Claim 161 (previously presented): The electrical circuit of claim 65, wherein said low voltage transistor is designed to operate in a saturation mode when propagating said analog signal.